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EXAMINER	
FLORES, LEON	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,964	PUKKILA ET AL.	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims (1 & 4-21) are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindoff et al (hereinafter Lindoff)(US patent 6,842,476 B2) in view of Bottomley (US Patent 5,822,380), and further in view of Skold et al (hereinafter Skold)(US Patent 5,933,768).**

Re claim 1, Lindoff discloses a method for suppression of interfering co-channel signals, synchronous or asynchronous, in a single antenna interference cancellation (SAIC) receiver by calculating a desired impulse response estimate signal (h ^ JCE (1)) ,comprising the steps of: receiving a radio signal by a receiver filter of the SAIC receiver and providing a filtered waveform signal (y) to a joint channel estimator of a

joint channel estimator module of the SAIC receiver (In Lindoff, see fig. 4: elements 10, 422 & 424, see col. 5, lines 29-33); computing the desired impulse response estimate signal (h ^ JCE (1))by the joint channel estimator using the filtered waveform signal (y), the desired bit decision signal (a(1)) and an interfering training sequence signal and an interfering training sequence delay signal generated without prior knowledge of a training sequence of the interfering co-channel signals. (In Lindoff, see col. 6, lines 29-34)

But the reference of Lindoff fails to specifically disclose providing a desired bit decision signal ((1)) to the joint channel estimator module. However, Bottomley does. (See fig. 3 & col. 6, lines 33-42)

Bottomley discloses a joint channel estimator which receives as input detected values, which are used by the joint channel estimator to generate channel tap coefficients estimates.

Therefore, taking the combined teachings of Lindoff & Bottomley as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated this step into the system of Lindoff, in the manner as claimed & and as taught by Bottomley, for the benefit of generating channel tap coefficients estimates. (In Bottmley, see col. 6, lines 1-4)

The combination of Lindoff & Bottomley, as discussed above shows the limitations claimed, except they do not specifically disclose that the interfering training sequence signal and an interfering training sequence delay signal are generated without prior knowledge of a training sequence of the interfering co-channel signals.

However, Skold does. (See abstract) Skold discloses an apparatus for estimating an interfering signal component portion of a received signal. The training sequence associated with the interfering signal component portion is determined without prior knowledge of the training sequence associated with such interfering signal.

Therefore, taking the combined teachings of Lindoff, Bottomley, & Skold as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Lindoff, as modified by Bottomley, in the manner as claimed and as taught by Skold, for the benefit of canceling the interfering signal from the received signal.

Re claim 4, the combination of Lindoff, Bottomley, & Skold further discloses that wherein the interfering signals are asynchronous with a desired signal. (In Lindoff, see col. 4, line 67 – col. 5, line 2)

Re claim 5, the combination of Lindoff, Bottomley, & Skold further discloses that wherein the interfering signals are synchronous with a desired signal. (In Lindoff, see col. 4, line 60)

Re claim 6, the combination of Lindoff, Bottomley, & Skold further discloses that wherein the desired bit decision signal ((1)) consists partly of a known training bit sequence signal. (In Bottomley, see col. 2, lines 4-35, including equation 4)

Re claim 7, the combination of Lindoff, Bottomley, & Skold further discloses that after receiving the radio signal by the receiver filter, further comprising the steps of: computing an initial desired impulse response estimate signal (.sub.CM) using the filtered waveform signal (y) by a channel estimator of a first stage of the SAIC receiver (In Bottomley, see fig. 2: the output of elements 26a & 26b); and computing (64) the desired bit decision signal ((1)) using the initial desired impulse response estimate signal (.sub.CM) and the filtered waveform signal (y) (In Bottomley, see fig. 2: the output of element by a single antenna interference cancellation (SAIC) detector of the first stage of the SAIC receiver. (In Lindoff, see fig.4)

Re claim 8, the combination of Lindoff, Bottomley, & Skold further discloses that wherein the channel estimator is an iterative constant modulus (CM) channel estimator and SAIC detector is a constant modulus single antenna interference cancellation (CM-SAIC) detector. (It is assumed that the power is constant in the modified system of Lindoff, Bottomley & Skold)

Re claim 9, the combination of Lindoff, Bottomley, & Skold further discloses that after the step of computing the desired impulse response estimate signal (h ^ JCE (1))by the joint channel estimator, further comprising the step of: computing a further desired bit decision signal ((2)) using the desired impulse response estimate signal (h ^ JCE (1))and the filtered waveform signal (y) by a further SAIC detector of a second stage of the SAIC receiver. (In Bottomley, see fig. 3: element 28. Furthermore, the

output of this system is iteratively fedback to the joint channel estimator and to the impairment correlation estimator for the purpose of estimating a second desired bit decision signal. Each of the iterations is considered to be a stage in the cancellation process.)

Re claim 10, the combination of Lindoff, Bottomley, & Skold further discloses that wherein the further desired bit decision signal ((2)) is an output signal of the SAIC receiver based on a predetermined criterion. (One skilled in the art would know that a iteration is terminated once a predetermined threshold or value has been reached.)

Re claim 11, the combination of Lindoff, Bottomley, & Skold further discloses providing the further desired bit decision signal ((2)) to a further joint channel estimator module of a third stage of the SAIC receiver. (In Bottomley, see fig. 3: 28. Furthermore, the output of this system is iteratively fedback to the joint channel estimator and to the impairment correlation estimator for the purpose of estimating a second desired bit decision signal. Each of the iterations is considered to be a stage in the cancellation process.)

Re claim 12, the combination of Lindoff, Bottomley, & Skold further discloses that wherein the channel estimator is an iterative constant modulus (CM) channel estimator and wherein the SAIC detector and the further SAIC detector are constant modulus

single antenna interference cancellation (CM-SAIC) detectors. (It is assumed that the power is constant in the modified system of Lindoff, Bottomley & Skold)

Claim 13 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 13. Therefore, claim 13 has been analyzed and rejected w/r to claim 1.

Claim 14 is a system claim corresponding to method claim 7. Hence, the steps performed in method claim 7 would have necessitated the elements in system claim 14. Therefore, claim 14 has been analyzed and rejected w/r to claim 7.

Claim 15 is a system claim corresponding to method claim 8. Hence, the steps performed in method claim 8 would have necessitated the elements in system claim 15. Therefore, claim 15 has been analyzed and rejected w/r to claim 8.

Claim 16 is a system claim corresponding to method claim 9. Hence, the steps performed in method claim 9 would have necessitated the elements in system claim 16. Therefore, claim 16 has been analyzed and rejected w/r to claim 9.

Claim 17 is a system claim corresponding to method claim 10. Hence, the steps performed in method claim 10 would have necessitated the elements in system claim 17. Therefore, claim 17 has been analyzed and rejected w/r to claim 10.

Claim 18 is a system claim corresponding to method claim 9. Hence, the steps performed in method claim 9 would have necessitated the elements in system claim 18. Therefore, claim 18 has been analyzed and rejected w/r to claim 9.

Claim 19 is a system claim corresponding to method claim 12. Hence, the steps performed in method claim 12 would have necessitated the elements in system claim 19. Therefore, claim 19 has been analyzed and rejected w/r to claim 12.

Claim 21 is a system claim corresponding to method claim 11. Hence, the steps performed in method claim 11 would have necessitated the elements in system claim 21. Therefore, claim 18 has been analyzed and rejected w/r to claim 11.

4. **Claims (2-3 & 20) are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindoff et al (hereinafter Lindoff)(US patent 6,842,476 B2), Bottomley (US Patent 5,822,380), & Skold et al (hereinafter Skold)(US Patent 5,933,768), and further in view of Suzuki et al (hereinafter Suzuki)(US Patent 6,088,383).**

Re claim 2, The method of claim 1, the combination of Lindoff, Bottomley, & Skold further discloses that after the step of providing the desired bit decision signal (a(1)) to the joint channel estimator module, further comprising the steps of: computing a replica signal calculated by a replica signal generation means of the joint channel estimator module as a convolution of the desired bit decision signal (a(1)) and a replica

impulse response h_r of said replica signal generation means; and (In Bottomley, see fig. 4 & col. 7, lines 12-45) generating a residual signal (i) by subtracting the replica signal from the filtered waveform signal y using an adder. (In Bottomley, see fig. 4 & col. 7, lines 46-54, including equations 7a & 7b)

But the combination of Lindoff, Bottomley, & Skold fails to specifically disclose a replica signal generation means. However, Suzuki does. (See fig. 4: 121 & col. 7, lines 55-60)

Suzuki discloses a replica generating means that generate replica of the respective spread spectrum signal contained in the received signal by re-spreading the correlations detected by the first correlation detecting means.

Therefore, taking the combined teachings of Lindoff, Bottomley, Skold & Suzuki as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Lindoff, as modified by Bottomley, Skold, as taught by Suzuki, for the benefit of generating replicas of the respective spread spectrum signals contained in the received signal.

Re claim 3, The method of claim 2, the combination of Lindoff, Bottomley, Skold, & Suzuki further discloses that wherein the interfering training sequence and the interfering training sequence delay signal are identified by calculating correlating signals of said residual signal (i) with the candidate training sequences or training sequences convolved by a known transmission pulse shape for all possible bit positions (In Bottomley, see fig. 4: 40 & col. 7, line 55 – col. 8, line 61); among said correlating

signals, the maximum correlation signal is selected as interfering training sequence (One skilled in the art would know that when determining the interfering training sequence one may compute it by correlating it with other training sequences and measuring their respective peaks.) and the corresponding timing position as the interfering training sequence delay signal which are provided to the joint channel estimator. (In Lindoff, see col. 6, lines 29-34)

Re claim 20, the combination of Lindoff, Bottomley, Skold, & Suzuki further discloses that wherein said joint channel estimator module comprises: a replica signal generation means, responsive to the desired bit decision signal ((1)), for providing a replica signal calculated by said replica signal generation means as a convolution of the desired bit decision signal (1) and a replica impulse response h.sub.r of said replica signal generation means **(This limitations has been analyzed and rejected w/r to claim 2 above.)**; an adder, for providing a residual signal by subtracting the replica signal from the filtered waveform signal (y) **(This limitation has been analyzed and rejected w/r to claim 2 above)**; a correlation means, responsive to the residual signal (), for providing the interfering training sequence and its delay signal identified by calculating correlating signals of said residual signal () with the candidate training sequences or training sequences convolved by a known transmission pulse shape for all possible bit positions; among said correlating signals, the maximum correlation signal is selected as the interfering training sequence signal and the corresponding timing position as the interfering training sequence delay signal which are provided to the joint

channel estimator **(This limitation has been analyzed and rejected w/r to claim 3 above)**; and a joint channel estimator, responsive to the filtered waveform signal (y), to the desired bit decision signal (1), to the interfering training sequence signal and to the interfering training sequence delay signal, for providing the desired impulse response estimate signal (h ^ JCE (1)). **(This limitation has been analyzed and rejected w/r to claim 2 above)**

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
March 5, 2007

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